

FIG. 2A

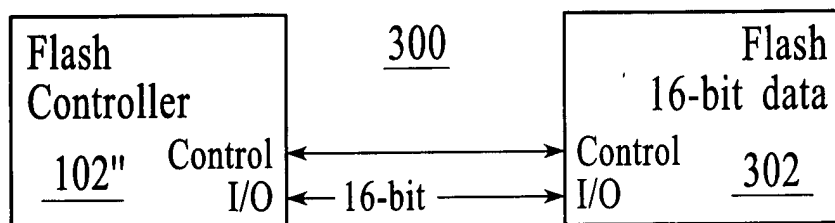


FIG. 2B

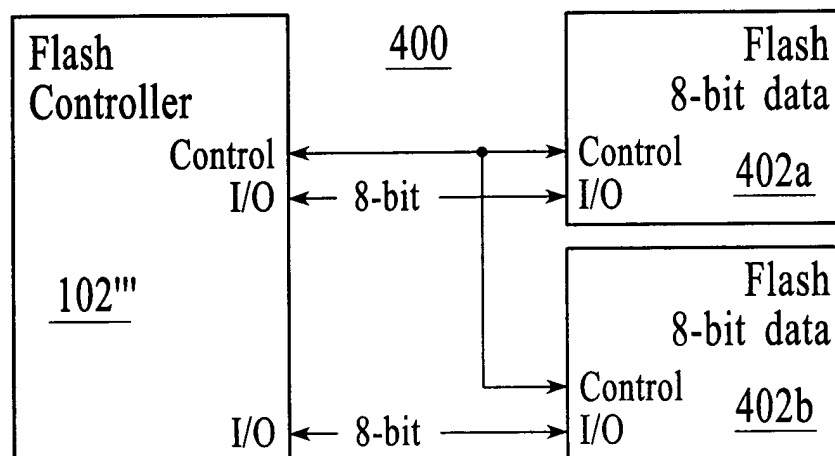


FIG. 2C

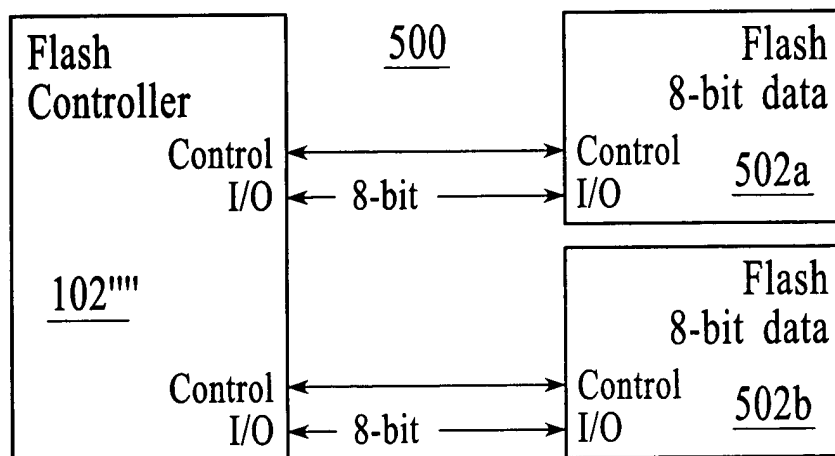


FIG. 2D

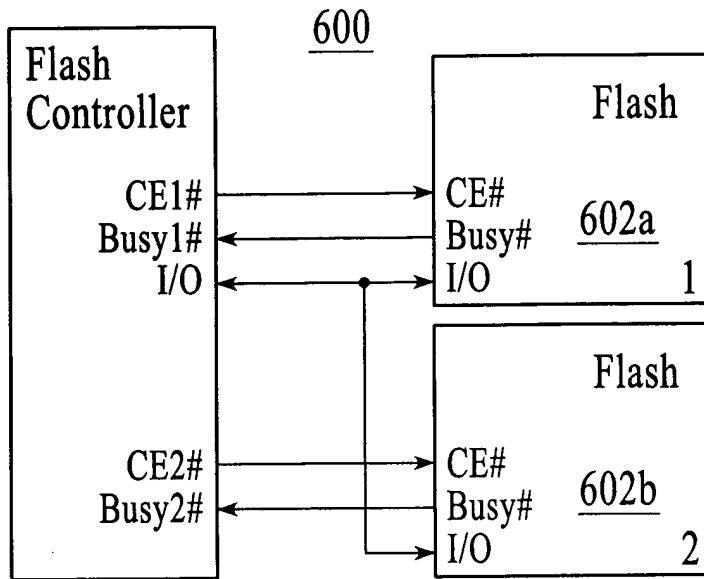


FIG. 3A

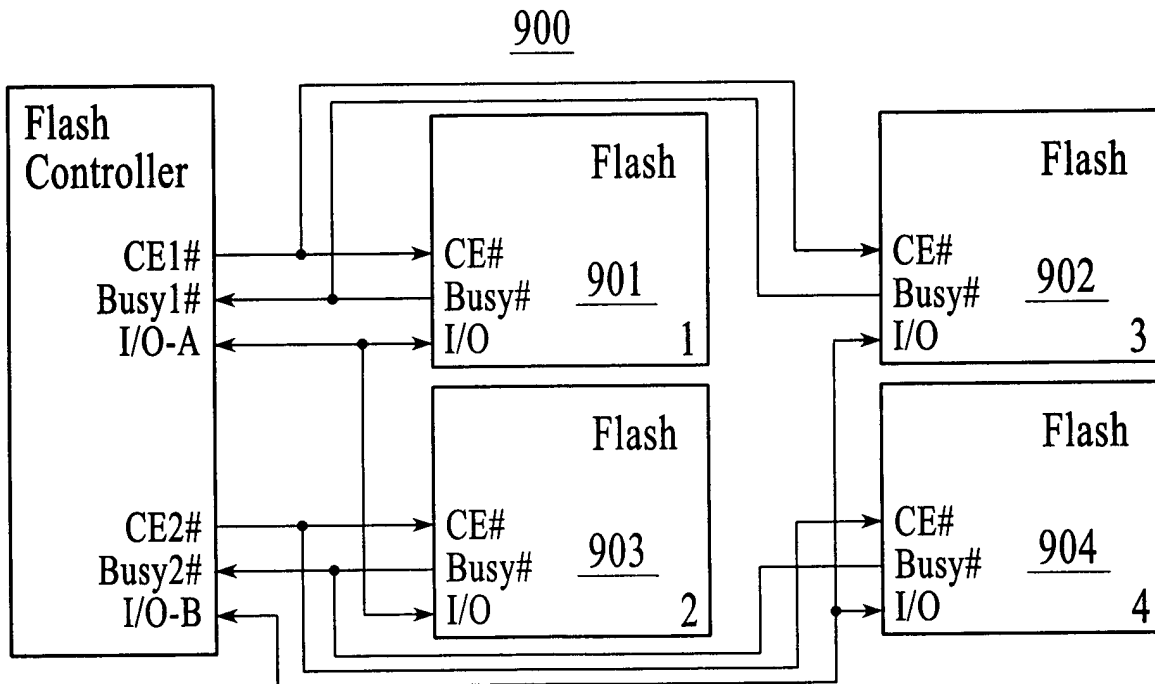


FIG. 3E

Acronym

- Ext Rd = External Read Data
- Ext Wc+ d = External Write Command and Data
- Int Rd = Internal Read Data
- Int Wd = Internal Write Data
- CE = Chip Enable

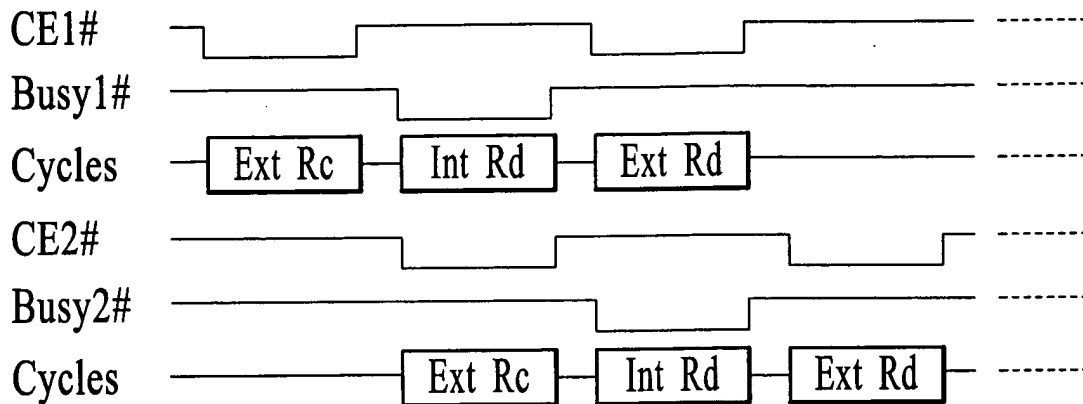


FIG. 3B

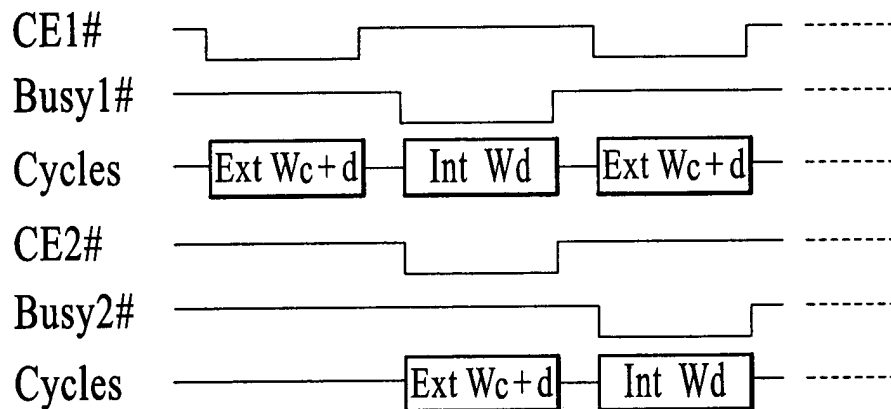


FIG. 3C

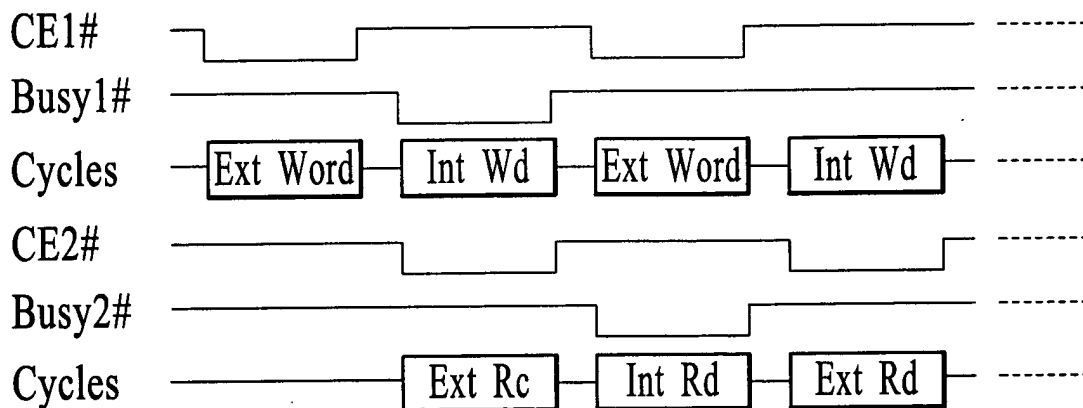


FIG. 3D

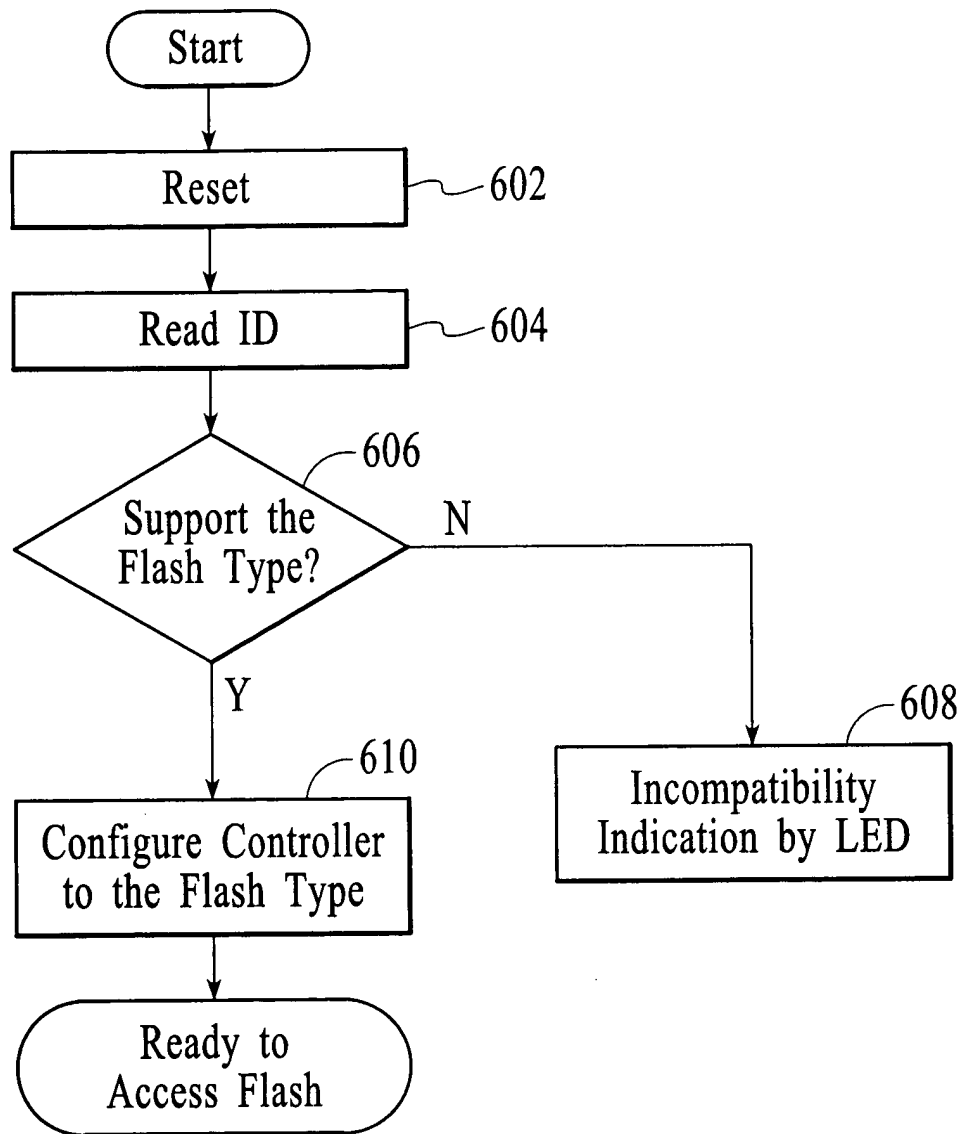


FIG. 4

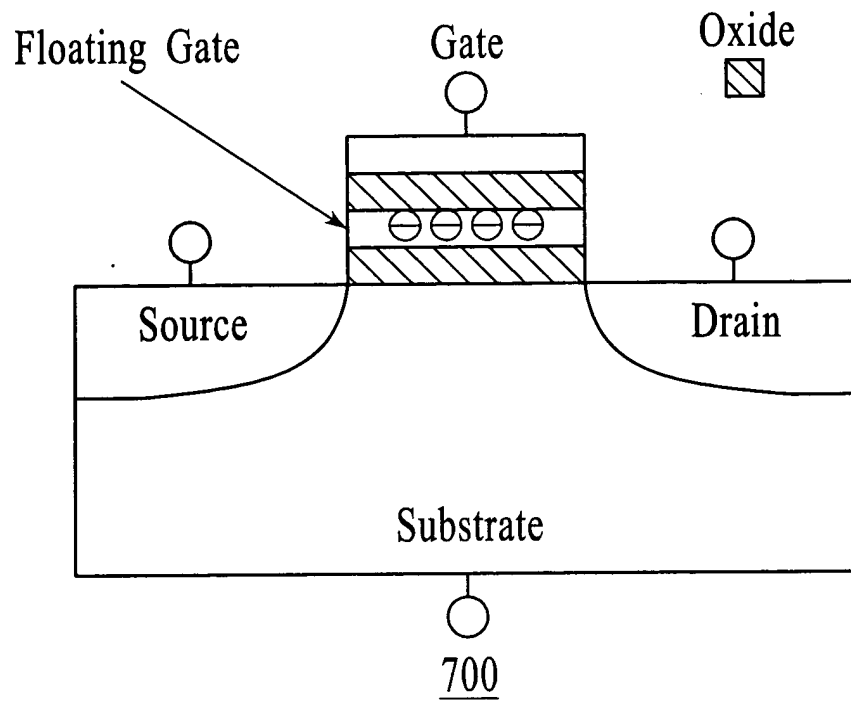


FIG. 5A

V_t	
0	Level 1
1	Level 0
SLC (1-bit/2-level)	

V_t	
00	Level 3
01	Level 2
10	Level 1
11	Level 0
MLC (2-bit/4-level)	

FIG. 5B

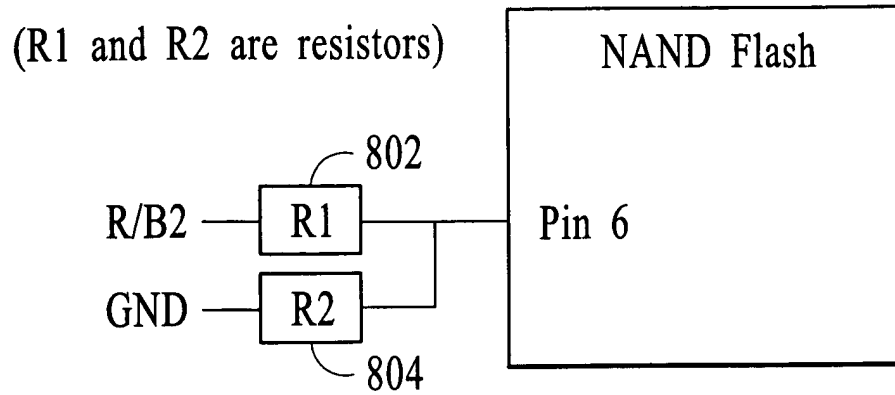


FIG. 6A

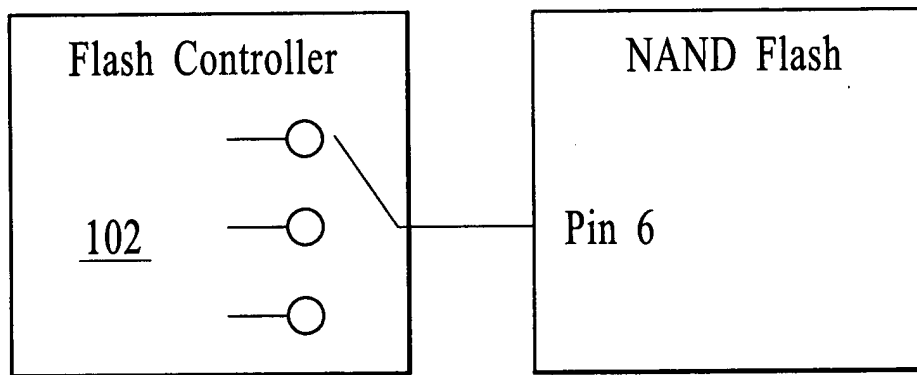


FIG. 6B

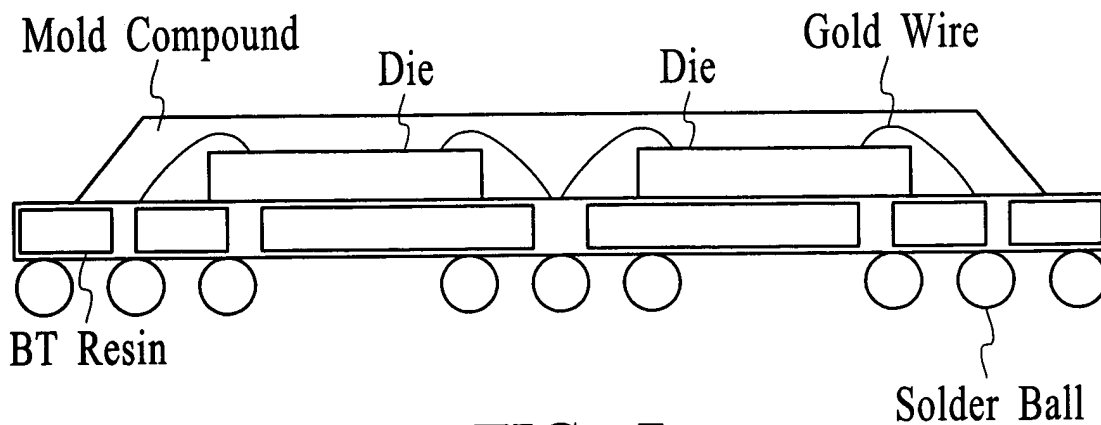


FIG. 7